Cadence Setup

ECE 09414 - 2 VLSI

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I. Introduction

This goal of this lab was to set up Cadence and to produce I-V curves for a PMOS and NMOS. These curves were produced through the use of Cadence and MobaXterm. MobaXterm was used to connect to the university’s server for use of Cadence. The I-V curves were produced using built in Cadence libraries and other features found within Cadence such as Spectre.

II. Procedure

Using MobaXterm a SSH connection to the Cadence server was established. With this connection the files used to configure and launch Cadence were brought into individual user files. Through the use of built in Cadence libraries such as “NCSU\_techlib\_ami06” the components needed to create the circuits for the I-V curves were imported. Through the use of Schematic XL files the circuits were created with “pmos4” and “nmos4” at the center. The I-V curve circuit for the NMOS transistor can be seen in Figure 1.1 and the circuit for the PMOS transistor can be seen in Figure 2.1. In each of these circuits two DC voltage supplies were used with varying voltages.

With the circuits complete the schematics were then used to create simulations in ADE GXL. Within the ADE GXL the variables were defined as sweeping voltages. The drain voltage, “vde”, was defined as sweeping from 0 to 2.5 in steps of 0.1. The output to be watched was defined at the positive terminal of DC voltage supply V3 for the NMOS transistor. Through parametric analysis with the gate voltage, “vgs”, stepping from 0 to 2.5 volts in steps of 0.25 the I-V was created. This I-V curve of the NMOS circuit can be seen in Figure 1.2. This process was repeated for the PMOS transistor with a difference in where the output was to be monitored. The output for the PMOS circuit was defined as the drain of the PMOS. With the same analysis parameters, barring the change in output, the I-V curve for the PMOS was created and can be seen in Figure 2.2.

III. Results

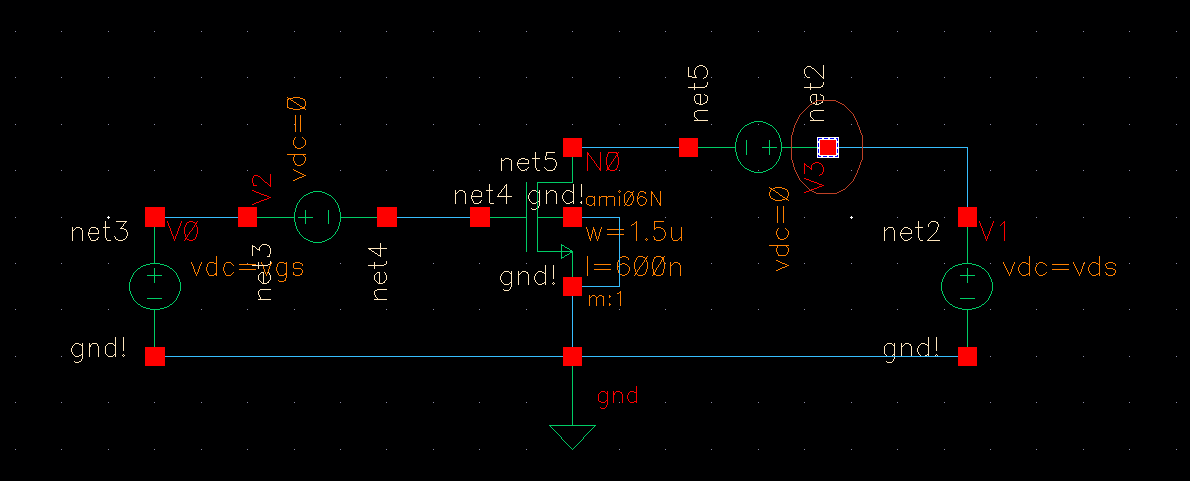


Figure 1.1: Schematic of NMOS circuit for I-V Curve.

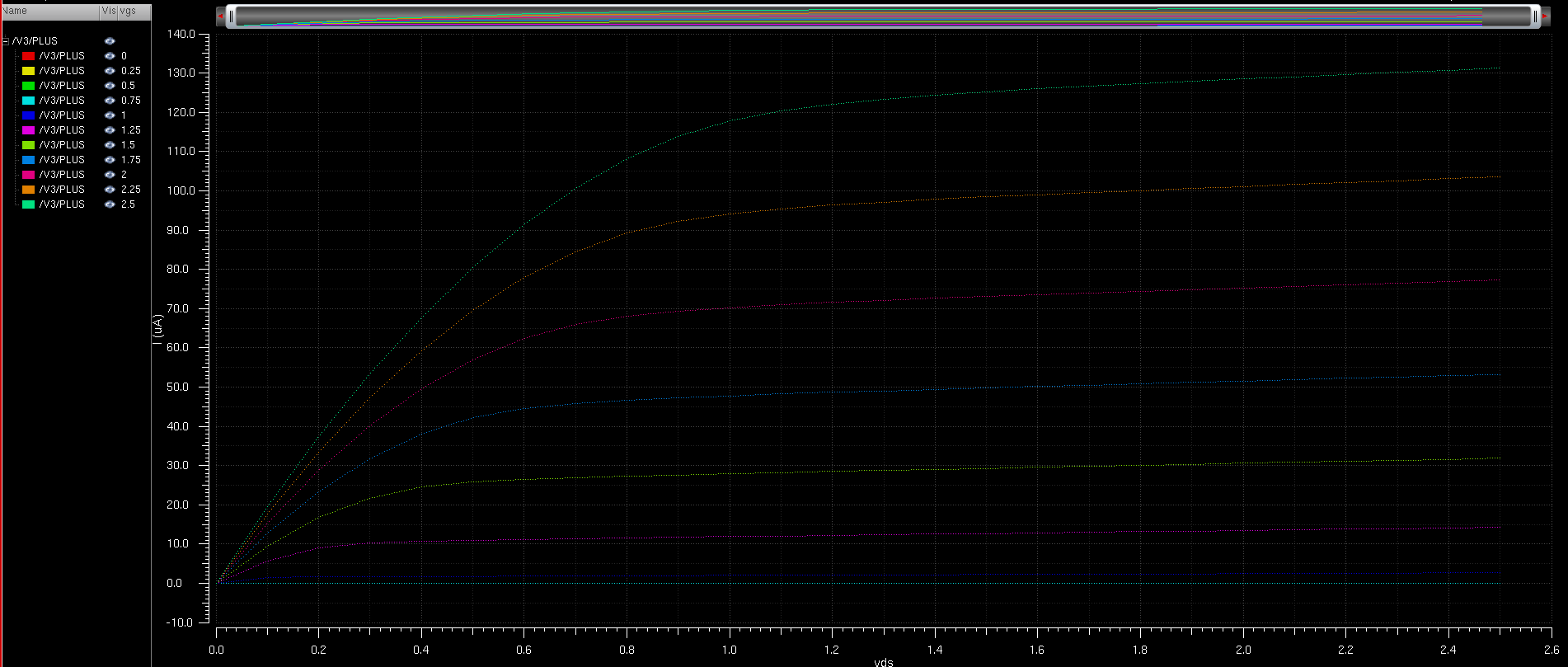


Figure 1.2: I-V curves of NMOS.

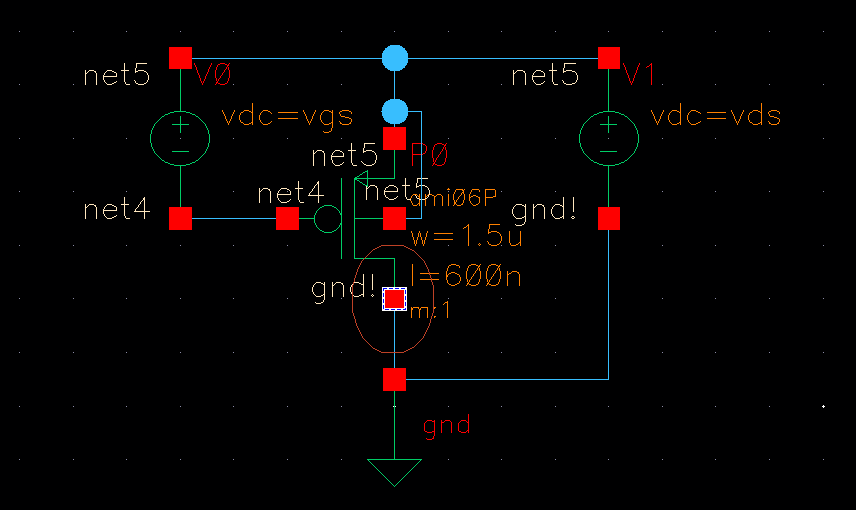


Figure 2.1: Schematic of PMOS circuit for I-V Curve.

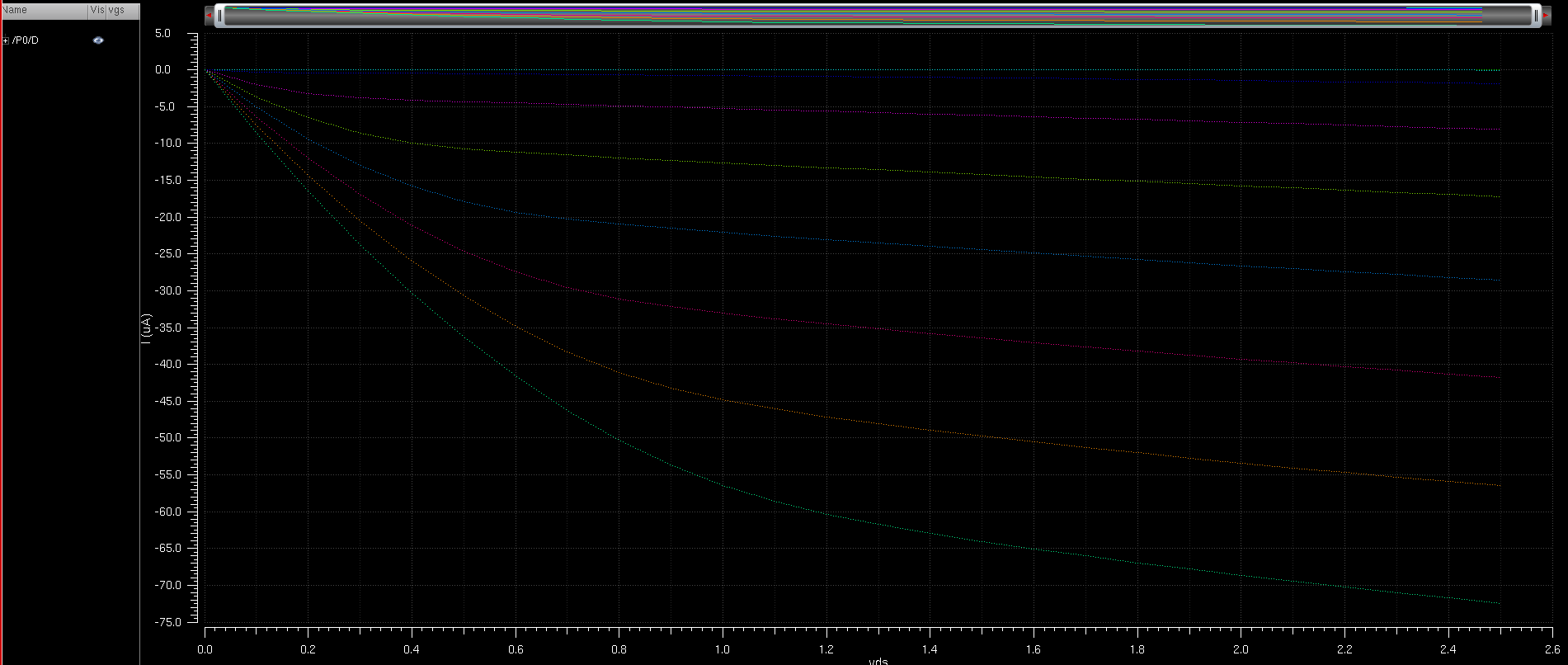


Figure 2.2: I-V curves of PMOS.

IV. Conclusions

From the lab procedure the I-V curves of both the NMOS and the PMOS were created with minor differences in the circuit design. With the creation of these graphs Cadence can be seen to be working properly as well. This would show that all goals for this lab procedure were met and done to their fullest.